3D stacked (foveros) SOC power delivery analysis methodology for predictable silicon success

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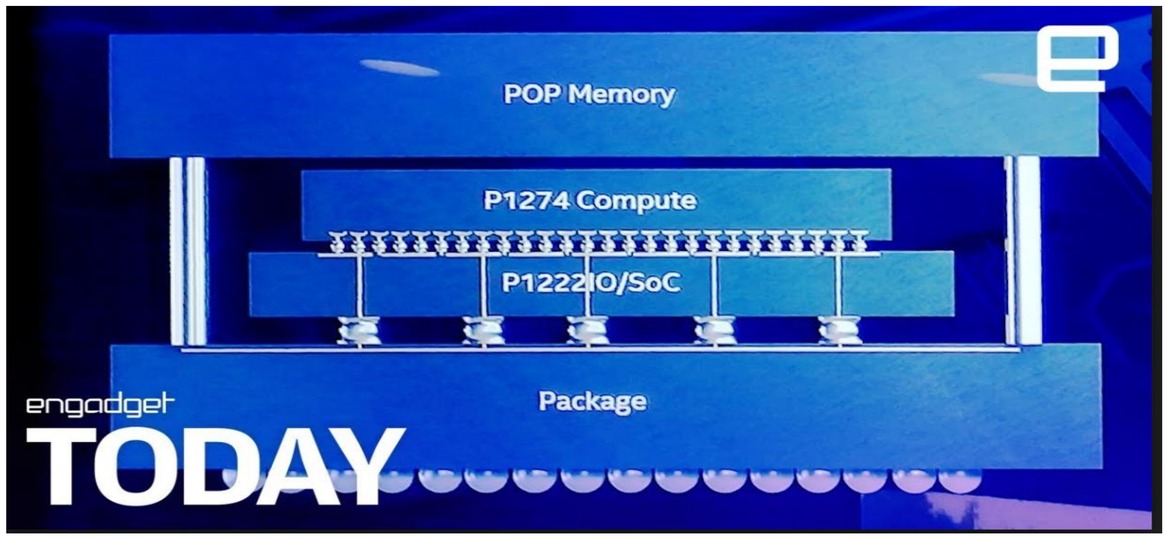
Intel Foveros technology is to stack computing circuits on top of each other and wire them together with speedy connections, enabling it to pack more onto a single chip.

Stacking has been used in memory chips before, but Intel would be the first company to successfully stack the so-called “logic” chips that handle computing tasks.

When multiple die stacks with through silicon via ,Top die power delivery is through bottom die stack. This poses immense challenge due to shared voltage rails and common ground across Dies.

The motivation is to share the methodology to analyze power delivery network of stacked die SOC, where power for compute pass through base die, having common shared rails between two dies and having common ground .



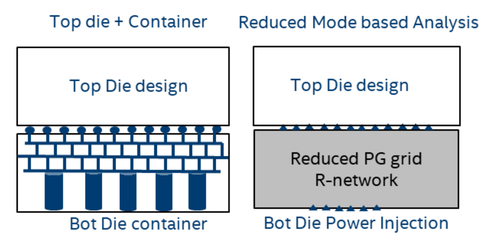
Foveros PDN challenges

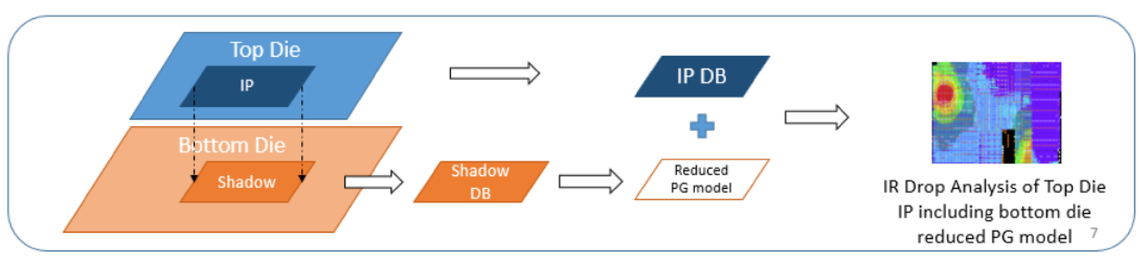
- Modeling of Through Silicon Via (TSV)
- Top die power delivery through bottom die
- Shared power rails and common ground across dies
- Die to die micro-bump connectivity
- EDA tool - Foveros is used first time in the industry for any production SOC, no vendor tool is available with proven silicon record

3D-IC Workflow

Early phase of the SOC design development cycle

- Bottom Die Containers created by cookie cut on shadow regions of Critical Top die IPs.
- PG network in container DB is modeled as reduced mxn multi-port R network
- Critical IP standalone runs included container reduced models to account for bottom die impact & voltage droop

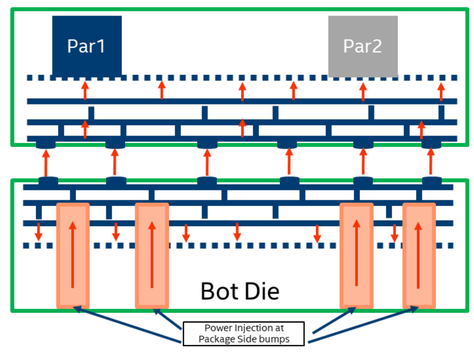


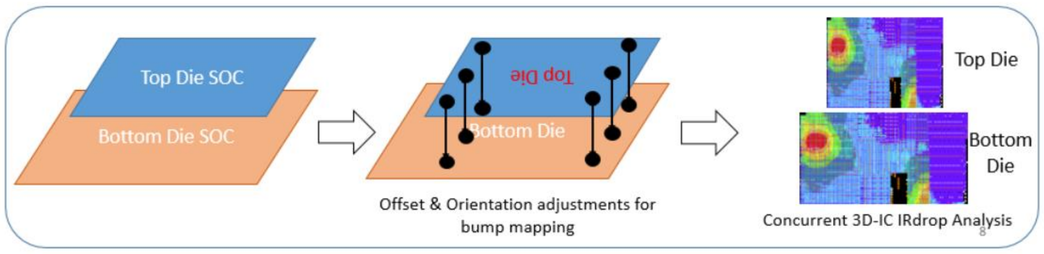


Later phase of the SOC design development cycle

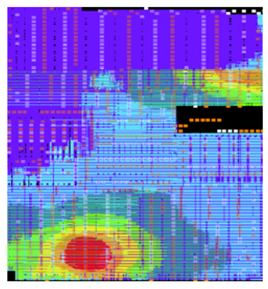
Concurrent dual-die analysis for power delivery check

- Individual Die runs to ensure intra-die robust connectivity from micro Bump to logic
- Concurrent 3D-IC voltage droop analysis with both die stitched together





Results



Red Area are hot spots and fixed using layout optimizations

- 3DIC PDN analysis flow and methodology developed.
- Two dies PDN network extracted in SOC context .
- The methodology is used for optimizing the TSV and PG grid .

3D IC based power delivery analysis helped to identify weaker spots

Summary and conclusions

- Concurrent analysis is a must for multi die stacking technology sharing voltage rails and common ground
- The described methodology helped to find out multiple design issues related to die to die connectivity weakness.
- It also helped optimizing the TSV count and PG grid .
- Separate strategy for early and signoff analysis helped the design to converge faster.

Highlight : Robust power delivery analysis methodology is developed to analyze stacked die SOC design, to find weaker spots and address those before tape-out to ensure that design meets the target power delivery network impedance and meets power supply noise requirements .

Acknowledgement

- Jai Prakash Sharma, Noel Pereira, Usha G M
- Sambit Sahu , Subhada Mishra, Anil Kempanna , Naren V .
- Wilfred Gomes, Arpan , Ajay , Rupesh , jai , Sunil , Shankar , Arun S, Silvian , Victor, Lei , Michael Z , Jonathan D , Noam , Dror , Sreekanth N .
- World wide Intel best in class technology team.